IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE paragraph [0061] with the following paragraph:

[0061] Other objects, features and advantages of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is an illustration of a conventional multiprocessor of a crossbar-interconnect type;

FIG.2 is an illustration of a multiprocessor according to a first embodiment of the present invention;

FIG.3 is a plan view of the multiprocessor shown in FIG.2;

FIG.4 is an illustration of a structure of a first back panel shown in FIG.2;

FIG.5 is an illustration of a variation of the first back panel shown in FIG.4;

FIG.6 is an illustration of a variation of a crossbar-board of the multiprocessor shown in FIG.3;

FIG.7 is an illustration of a multiprocessor according to a second embodiment of the present invention;

FIG.8 is an illustration of a multiprocessor according to a third embodiment of the present invention;

FIG.9 is an illustration of a multiprocessor according to a fourth embodiment of the present invention;

FIG.10 is an illustration of a multiprocessor according to a fifth embodiment of the present invention;

FIG.11 is a side view of the multiprocessor shown in FIG.10 and Fig. 11-1 is an enlarged view of the structure illustrated in the circled portion of the side view of Fig. 11;

FIG.12 is an illustration of a multiprocessor according to a sixth embodiment of the present invention;

FIG.13 is an illustration of a multiprocessor according to a seventh embodiment of the present invention;

FIG.14 is an illustration of a multiprocessor according to an eighth embodiment of the present invention;

FIG.15 is a magnified illustration of a connecting part of an extension crossbar-board and a crossbar-board shown in FIG.14 and FIGS. 15-1 and 15-2 are enlarged views of the corresponding circled portions of the structure illustrated in FIG. 15;

FIG.16 is an illustration of a multiprocessor according to a ninth embodiment of the present invention;

FIG.17 is an illustration of a multiprocessor according to a tenth embodiment of the present invention;

FIG.18 is an illustration for explaining a process of assembling a multiprocessor when the multiprocessor comprises a single back panel;

FIG.19 is an illustration of a multiprocessor according to an eleventh embodiment of the present invention;

FIG.20 is an illustration of a multiprocessor according to a twelfth embodiment of the present invention;

FIG.21 is an illustration of a first variation of a crossbar board-back panel assembly shown in FIG.20;

FIG.22 is an illustration of a second variation of the crossbar board-back panel assembly shown in FIG.20;

FIG.23 is an illustration of a multiprocessor according to a thirteenth embodiment of the present invention;

FIG.24 is an illustration of a first connection part on each of small panels shown in FIG.23;

FIG.25 is an illustration of a first variation of the first connection part shown in FIG.24;

FIG.26 is an illustration of a second variation of the first connection part shown in FIG.24;

FIG.27 is an illustration of a multiprocessor according to a fourteenth embodiment of the present invention;

FIG.28 is an illustration of a multiprocessor according to a fifteenth embodiment of the present invention;

FIG.29 is an illustration of a multiprocessor according to a sixteenth embodiment of the present invention;

FIG.30 is an illustration of a multiprocessor according to a seventeenth embodiment of the present invention;

FIG.31A is a perspective view showing a first assembling method of a crossbar board-

back panel assembly shown in FIG.2;

FIG.31B is a side view showing the first assembling method of the crossbar board-back panel assembly shown in FIG.2;

FIG.32A is a perspective view showing a second assembling method of the crossbar board-back panel assembly shown in FIG.2;

FIG.32B is a side view showing the second assembling method of the crossbar board-back panel assembly shown in FIG.2;

FIG.33 is an illustration of a first variation of the crossbar board-back panel assembly shown in FIG.2;

FIG.34 is an illustration of a second variation of the crossbar board-back panel assembly shown in FIG.2;

FIG.35A is an illustration of a third variation of the crossbar board-back panel assembly shown in FIG.2;

FIG.35B is an illustration of a server including a room to contain the crossbar board-back panel assembly shown in FIG.35A;

FIG.35C is an illustration of the server shown in FIG.35B containing the crossbar board-back panel assembly shown in FIG.35A in the room;

FIG.36A is an illustration of the crossbar-board being connected to the first back panel, of a fourth variation of the crossbar board-back panel assembly shown in FIG.2;

FIG.36B is a cross-sectional view of a connection pin shown in FIG.36A before being inserted into a connection block;

FIG.36C is a cross-sectional view of the connection pin shown in FIG.36A inserted into the connection block;

FIG.36D is a cross-sectional view of the connection pin shown in FIG.36A bending upward in the connection block;

FIG.37 is an illustration of a fifth variation of the crossbar board-back panel assembly shown in FIG.2;

FIG.38 is an illustration of a connection part of the crossbar-board and the first back panel, of a sixth variation of the crossbar board-back panel assembly shown in FIG.2;

FIG.39 is an illustration of a connection part of the crossbar-board and the first back panel, of a seventh variation of the crossbar board-back panel assembly shown in FIG.2;

FIG.40 is an illustration of an eighth variation of the crossbar board-back panel assembly shown in FIG.2; and

FIG.41 is an illustration of a ninth variation of the crossbar board-back panel assembly

shown in FIG.2.

Please REPLACE paragraph [00138] with the following paragraph:

[00138] FIG.10 is an illustration of a multiprocessor 50E according to a fifth embodiment of the present invention. FIG.11 is a side view of the multiprocessor 50E shown in FIG.10 and Fig. 11-1 is an enlarged view of the structure illustrated in the circled portion of the illustration of Fig. 11. The multiprocessor 50E is an SMP (Symmetric Multiprocessor) of the crossbar-interconnect type. In the multiprocessor 50E, the crossbar-boards are connected to the back panels by connecters facing different directions than in the multiprocessor 50 shown in FIG.2.

Please REPLACE paragraph [00159] with the following paragraph:

[00159] The stacking connector 240, best seen in the enlarged view of Fig. 15-1, comprises: a flat-cable unit 241; stacking male-connectors 242 and 243 respectively attached on both ends of the under surface of the flat-cable unit 241, best seen in the enlarged view of Fig. 15-2; a stacking female-connector 244 attached on one end of the upper surface of the extension crossbar-board 231; and a stacking female-connector 245 attached on one end of the upper surface of the board 61. The stacking male-connectors 242 and 243 are connected to the stacking female-connectors 244 and 245, respectively.